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Silicon Errata for the CY8C21x34 PSoC® Mixed Signal Arrays

This document describes the errata for the PSoC® Mixed Signal Arrays CY8C21x34. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21x34	CY8C21234-24SXI
	CY8C21234-24SXIT
	CY8C21334-24PVXI
	CY8C21334-24PVXIT
	CY8C21534-24PVXI
	CY8C21534-24PVXIT
	CY8C21434-24LFXI
	CY8C21434-24LFXIT
	CY8C21434-24LKXI
	CY8C21434-24LKXIT
	CY8C21634-24LFXI
	CY8C21634-24LFXIT
	CY8C21434-24LTXI
	CY8C21434-24LTXIT
	CY8C21434-24LQXI
	CY8C21434-24LQXIT
	CY8C21634-24LTXI
	CY8C21634-24LTXIT
	CY8C21001-24PVXI

CY8C21x34 Qualification Status

Product Status: Production

CY8C21x34 Errata Summary

The following table defines the errata applicability to available CY8C21x34 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C21x34	A	Silicon fix is planned.

1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **PROBLEM DEFINITION**

  Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70°C. This problem does not affect end-product usage between 0 and 70°C.

- **PARAMETERS AFFECTED**

  The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70°C and within the upper and lower datasheet temperature range is ±5%.

- **TRIGGER CONDITION(S)**

  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70°C.

- **SCOPE OF IMPACT**

  This problem may affect UART, IrDA, and FSK implementations.

- **WORKAROUND**

  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

- **FIX STATUS**

  The cause of this problem and its solution has been identified. Silicon fix is planned to correct the deficiency in silicon.

References

[1] Document # 38-12025, CY8C21234/CY8C21334/CY8C21434/CY8C21534/CY8C21634 PSoC® Mixed-Signal Array Final Data Sheet

[+] Feedback

Document History Page

Document Title: Silicon Errata for the CY8C21x34 PSoC® Mixed Signal Arrays Document Number: 001-48789				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	2567361	09/16/08	XSG/AESA	IMO tolerance deviation

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Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com

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